## **Refine Search**

#### Search Results -

Term	Documents
INTERCONNECT	71291
INTERCONNECTS	40102
DRAM	43785
DRAMS	9236
CHIP	188859
CHIPS	93926
SCALAR	10444
SCALARS	971
VECTOR	131350
VECTORS	87226
(SCALAR AND DRAM AND INTERCONNECT AND CHIP AND VECTOR).CLMPGPB.	0
((INTERCONNECT AND DRAM AND CHIP AND SCALAR AND VECTOR).CLM.).PGPB.	0

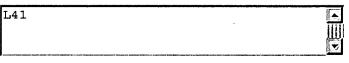
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### Search History

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DB =	PGPB; PLUR=YES; OP=OR		
L41	(interconnect and DRAM and chip and scalar and vector).clm.	0	<u>L41</u>
	PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	· ·	<u> </u>
L40	L39 and l1	18	L40
L39	(sushma or bratt or benkual or iwamoto or vaughn).in.	25306	<u>L39</u>
	23300	<u> </u>	
L38	PGPB; PLUR=YES; OP=OR  (sushma or bratt or benkual or iwamoto or vaughn).in.	1145	L38
	(interconnect and DRAM and controller\$1 and chip and scalar and		
<u>L37</u>	vector).clm.	0	<u>L37</u>
<u>L36</u>	((ic or integrated) and coheren\$5 and DRAM and controller\$1 and chip and scalar and vector).clm.	0	<u>L36</u>
<u>L35</u>	((ic or integrarted) and coheren\$5 and DRAM and controller\$1 and chip and scalar and vector).clm.	0	<u>L35</u>
<u>L34</u>	L33	0	<u>L34</u>
DB =	PGPB,USPT,USOC; PLUR=YES; OP=OR		
<u>L33</u>	((ic or integrarted) and coheren\$5 and DRAM and I near1 O near3 controller\$1 and chip and scalar and vector).clm.	0	<u>L33</u>
DB =	PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
<u>L32</u>	L28 and 115	2	<u>L32</u>
<u>L31</u>	L28 and 114	3	<u>L31</u>
<u>L30</u>	L28 and 113	19	<u>L30</u>
<u>L29</u>	L28 and l12	29	<u>L29</u>
<u>L28</u>	15 and (host\$3 or DRAM or ram)	74	<u>L28</u>
DB =	PGPB,USPT; PLUR=YES; OP=OR		
<u>L27</u>	110 and 115	0	<u>L27</u>
<u>L26</u>	110 and 114	1	<u>L26</u>
<u>L25</u>	110 and 113	62	<u>L25</u>
<u>L24</u>	110 and 112	121	<u>L24</u>
<u>L23</u>	19 and 115	1	<u>L23</u>
<u>L22</u>	19 and 114	1	<u>L22</u>
<u>L21</u>	19 and 113	26	<u>L21</u>
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<u>L17</u>	15 and 113	19	<u>L17</u>
<u>L16</u>	15 and 112	36	<u>L16</u> .
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<u>L13</u>	(712/3-38, 225-228)[CCLS]	4772	<u>L13</u>
<u>L12</u>	(712/2-300)[CCLS]	13531	<u>L12</u>
	PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
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<u>L6</u>	L5 and 13	18	<u>L6</u>
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<u>L4</u>	(south or north) near45 (bridge or interconnect\$4 or crossbar\$1 or switch\$3 or gate\$1 or rout\$4)	15523	<u>L4</u>
<u>L3</u>	coheren\$4 near15 (memor\$4 or stor\$4 or cach\$4)	15446	<u>L3</u>
<u>L2</u>	coheran\$4 near15 (memor\$4 or stor\$4 or cach\$4)	7	<u>L2</u>
<u>L1</u>	(chip or chipset or interconnect\$3 or ic) and (vector) and scalar	7016	<u>L1</u>

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IET CNF IET	Conference Proceeding	<u> </u>		chip provides real	-time video process	sing economically and e	fficiently
IEEE STD IEEE	E Standard		Morton, S.G.; ELECTRO '96, Profe	essional Program. F	Proceedings.		
			30 April-2 May 1996 Digital Object Identifi				
			AbstractPlus   Full To	ext: <u>PDF</u> (628 KB)			
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		2.	Araki, T.; Toyokura,	M.; Akiyama, T.; Ta	akeno, H.; Wilson, B.		
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